

REMARKS

Applicants respectfully traverse and request reconsideration

The drawings have been objected to, in particular, Figures 1 and 3 due to overlapping text with figure elements. Applicants submit corrected and formal replacement drawings for Figures 1 and 3.

The Abstract has been objected to as being too long. Applicants have also corrected this. This objection is respectfully requested to be withdrawn.

Claims 4-5, 8, 10-11, 13, 15-16 and 18 are objected to because of typographical errors. Applicants have amended the claims to correct typographical errors and respectfully request that this objection be withdrawn.

Claims 1-18 stand rejected under 35. U.S.C. §103(a) as being unpatentable over Applicants' admitted prior art in view of U.S. Patent No. 6,067,272 (Foss et al.). The Foss reference is directed to a delayed lock loop implementation in a synchronous dynamic random access memory. The Foss reference does not appear to be directed to nor contemplate problems associated with STROBE signals and double data rate communication systems. Applicants have amended the claims to more distinctly note the claims are directed to systems that employ the STROBE signal, such as in double data rate communication systems.

In addition, the Office Action rejects the claims based on the combination of Applicants' admitted prior art and the teachings of Foss. As noted above, the Foss reference does not contemplate or appear to consider any problems relating to the synchronization of STROBE signals nor to use of voltage controlled delay lines. In addition, Applicants' admitted prior art did not provide any description of how to solve problems being faced by those employing the prior art nor does Foss appear to provide any solution on how to address the issues set forth in Applicants' disclosure and solved by Applicants' claimed invention.


For example, with respect to independent claims 1, 9 and 14, for example, neither Applicants' prior art nor the Foss reference describe a variable delay circuit that receives a STROBE signal that's operatively responsive to a delay control signal to provide a phase-shifted STROBE signal as an output signal and that also utilizes a reference signal dividing circuit that receives the clock signal and a feedback control signal, along with the feedback delay matching array, coupled to the delay lock loop that produces a feedback control signal. As such, Applicants respectfully submit that the claims are in condition for allowance. As noted in Applicants' specification, Applicants' invention can provide among other advantages, a one quarter STROBE phase shift and adds, for example, four multiplexers and another four buffers to the delay lock closed loop path. Likewise to shift the STROBE signal by half of the clock period, the DLL may include two multiplexers and two buffers in the closed loop path. The Foss reference does not appear to contemplate attempting to solve the same problem with respect to the STROBE signal that is described in Applicants' claimed invention. In addition, Applicants have added claims 19 and 20 to further cover this structure.

The dependent claims add additional novel and non-obvious subject matter and therefore these claims are also believed to be in condition for allowance.

As to new claims 19 and 20, Applicants respectfully submit that the Foss reference and Applicants submitted prior art are silent as to the number of multiplexers and buffers that are serially coupled as a function of the fraction of the reference clock period to be adjusted.

Accordingly, Applicants respectfully request that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

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